ABSTRACT OF THE DISCLOSURE

A SDH test apparatus substitutes a part of payload of received SDH data with a desired data and transmits. A FIFO memory is installed between the Rx AU processor and the Tx AU processor, stores sequentially AU data extracted by the Rx AU processor and outputs to the Tx AU processor in the order of memorization. An AU pointer processor outputs an AU pointer adjusting the number of data in the FIFO memory, allowing the Tx AU processor to read in payload of AU data, after a time lag ($\Delta T2 + \Delta T4$) of information leading head position of payload generated by the processing of AU data by the Rx AU processor and the Tx AU processor, by extracting the number of data in the FIFO memory. The Tx AU processor is composed to read out the payload of AU data from the FIFO memory, generate AU data and output to the Tx SOH processor so that the information leading position is at the position designated by the AU pointer value output from the AU pointer processor.